Examiner Thomas L. Dickey is thanked for having thoroughly examined the present invention.

The specification has been amended to include a brief description of Figure 2m, which was added in response to the first office action. It is believed that the objection to the specification has been overcome, and it is so requested, respectfully.

Reconsideration of the rejection of claim 1 under 35 USC 102(e) as being anticipated by Lam, et al., (6,445,029) is respectfully requested in view of the amendments and for the reasons given below.

The cited reference discloses a floating gate 34 provided with "an upward edge 12 and two downward pointing edges 14," as indicated in Fig. 2B, and column 3, lines 62-64. However, the top surface of the floating gate in the same figure is flat, and so are the control gate 38 and the intervening oxide 36. A main feature and key aspect of the present invention, on the other hand, is to provide several layers of "folded" surfaces (fourth line from the bottom of page 14) starting from the top surface of floating gate

120, and propagating conformally upwards through oxide layers 160, 170, including both the bottom and top surfaces of control gate 180. Although Fig. 3G of the reference shows irregular surfaces, they do not replicate conformally the "edges 12 and 14."

More importantly, the floating gate 34 of the reference has a bottom surface, which is also irregular, and the irregularity dips into the substrate (please see Figures 2B and 3E-3G). In contrast, the bottom surface of floating gate 120 of the instant invention (please see Figures 2a-2m) not only is flat, but also separated from the substrate by intervening gate-oxide layer 110. That is, the structures of the reference are different from that of the instant invention. In order to distinguish the present invention from the reference even more, claim 1 has been amended to cite the flat bottom of the floating gate in conformance with the amendment to the specification with no new matter added. It is believed that claim 1 is allowable, and it is so requested, respectfully.

Reconsideration of the rejection of claims 2, 3, 5 and 6 under 35 USC 103(a) as being unpatentable over Lam,

et al., (6,445,029) is respectfully requested in view of the amendments and for the reasons given below.

In view of the amendments and reasons given above, it is believed that claim 1 is allowable, and hence, claims 2, 3, 5 and 6 dependent from claim 1, and it is so requested, respectfully.

Allowance of all claims, as amended, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. the attached page is captioned **"Version with Marking to Show Changes Made."**

It is requested that should the Examiner not find that the Claims Allowable that are now presented, that he call the undersigned Attorney at 845/452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 14, the last paragraph has been amended as follows:

As a main feature and key aspect of the present invention, etching is continued further with gases $HBr+Cl_2$ to form step (125) in first polysilicon layer (120) as shown in Fig. 2f. For a step depth of preferably between about 900 to 1100 Å, the added surface area on the first polysilicon layer is between about 20 to 40 % where the higher 40% is preferred. This increase is also reflected in the increased capacitance and therefore in the increased coupling ratio between the floating gate and the control gate to be formed conformally over the floating gate. It will be observed that the top surface of the first polysilicon layer exposed in (125) can be "folded" several times over by having several steps or "fins" similar to that is found in heat sinks. Furthermore, the fins can comprise other shapes, such as triangular, or trapezoidal,

and so on, all designed to increase the [surface] area of the top surface of the first polysilicon layer (120). As another key step, additional area is gained by removing oxide spacers (155) to expose additional polysilicon areas underneath the spacers, as seen in Fig. 2g.

IN THE CLAIMS

The following claims have been amended as follows:

1. (TWICE AMENDED)A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of different shapes comprising:

a semiconductor substrate;

a floating Poly-Si gate with multiply connected top surface having regions of different cross-sectional shapes ,said Poly-Si gate having a flat bottom surface;

wherein said cross-sectional shapes are selected from a group consisting of rectangular and triangular shapes;

[an] a conformal inter-poly dielectric layer replicating said shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said shapes over said inter-poly dielectric layer.